Notice of Allowability	Application No.	Applicant(s)		
	09/531,860	FIGUEREDO, JORG	FIGUEREDO, JORGE HUMBERTO	
	Examiner	Art Unit		
	Jeffrey R. West	2857		
The MAILING DATE of this communication appeal claims being allowable, PROSECUTION ON THE MERITS IS herewith (or previously mailed), a Notice of Allowance (PTOL-85) NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIOF the Office or upon petition by the applicant. See 37 CFR 1.313	(OR REMAINS) CLOSED in or other appropriate commits (GHTS). This application is	n this application. If not include unication will be mailed in due of	d course. THIS	
 This communication is responsive to the Amendment filed The allowed claim(s) is/are 10. The drawings filed on 20 November 2003 are accepted by Acknowledgment is made of a claim for foreign priority una)	the Examiner. nder 35 U.S.C. § 119(a)-(d)	or (f).		
1. Certified copies of the priority documents have				
2. Certified copies of the priority documents have	• • • • • • • • • • • • • • • • • • • •			
3. Copies of the certified copies of the priority doc	cuments have been receive	d in this national stage applicati	on from the	
International Bureau (PCT Rule 17.2(a)).				
* Certified copies not received: 5. Acknowledgment is made of a claim for domestic priority ur reference was included in the first sentence of the specifica (a) The translation of the foreign language provisional a claim for domestic priority ur in the first sentence of the specification or in an Application or the first sentence of the specification or in an Application or	ation or in an Application Data pplication has been received ander 35 U.S.C. §§ 120 and/or Data Sheet. 37 CFR 1.78. If this communication to file at this application. THIS THE attached EX are reason(s) why the oath of the submitted. Son's Patent Drawing Review or rection filed, which is Amendment / Comment of the submitted, which is a factor of the submitted	ata Sheet. 37 CFR 1.78. add. for 121 since a specific reference a reply complying with the requil REE-MONTH PERIOD IS NOT BE AMINER'S AMENDMENT or NO ar declaration is deficient. W (PTO-948) attached The has been approved by the Exer in the Office action of Paper New The drawings in the front (not the I	e was included rements noted EXTENDABLE. OTICE OF aminer.	
9. DEPOSIT OF and/or INFORMATION about the deposit DEPOSIT OF and/or INFORMATION about the deposit attached Examiner's comment regarding REQUIREMENT FOR TI	HE DEPOSIT OF BIOLOGI		ote the	
Attachment(s)	* *	9		
Notice of References Cited (PTO-892)	5☐ Notice of Infe	ormal Patent Application (PTO-1	152)	
 Police of Draftperson's Patent Drawing Review (PTO-948) Information Disclosure Statements (PTO-1449 or PTO/SB/08 Paper No 		6☐ Interview Summary (PTO-413), Paper No		
), 7☐ Examiner's /	Amendment/Comment		
Examiner's Comment Regarding Requirement for Deposit of Biological Material	8⊠ Examiner's 9 Dther	Statement of Reasons for Allowa	ance	

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DETAILED ACTION

Allowable Subject Matter

1. Claim 10 is considered to be allowable over the cited prior art for the following reasons:

ESPEC Technology Report, "Special issue: Evaluating Reliability and Measurement System" teaches a method for testing a multi-chip IC package as a device under test, using temperature cycle testing in order to test for intermittent cracks, which lead to disconnection (i.e. open circuits) in its internal components (page 12, column 1, lines 18-39) comprising applying a rising temperature to the device under test while concurrently measuring the resistance during an up temperature ramp, at regular intervals, reducing down the temperature of the device under test back to starting room temperature while monitoring and reading the resistance, at regular intervals, plotting a graph of the resistance of the device during the temperature up ramp and during the temperature down ramp, and noting an erratic irregularity of the resistance plotted on a computer screen against temperature graphs in order to determine the intermittent defectiveness of components within the multi-chip package clearly distinguishable from a normal set of components (i.e. sample a vs. sample b) (page 12, column 2, lines 31-47 and Figure 6). ESPEC also teaches determining the resistance using an ohmmeter (i.e. a device functionally equivalent and obviously exchangeable for a multi-meter), connected through an I/O socket (page 13, Figure 7). Further, since the invention shows that the resistance of the device under test returns to its original value when

the temperature is returned to room temperature (Figure 6), the invention of ESPEC teaches non-destructive testing of the device for intermittent faults.

U.S. Patent No. 5,107,325 to Nakayoshi teaches a packaged semiconductor device wherein the device is tested using temperature cycle tests that cause thermal stress due to a difference in the linear coefficient of expansion between semiconductor chips and the printed wiring board (column 3, lines 11-16). Nakayoshi also teaches performing the temperature cycle test in order to determine a plurality of deteriorations such as cracks, disconnection (i.e. open circuits), and short-circuits (column 7, lines 28-58).

JP Patent No. 10-239373 to Agawa teaches a short circuit checker used in packaging parts of printed circuit boards comprising attaching the printed circuit base to a test socket (0007) and monitoring the resistance between the power supply line (i.e. power bus) and common line (i.e. ground) in order to determine the occurrence of a short circuited, faulty component (0004) which is indicated by a non-linear, rapid change in resistance (0009).

U.S. Patent No. 5,419,780 to Suski teaches a method and apparatus for recovering power from a semiconductor circuit using a well known Peltier-junction thermoelectric heat-reducing cooler which generates a temperature differential between two opposing surfaces (column 4, lines 59-62) wherein one of the surfaces is conductively connected, such as with a metallic shield or adhesive (i.e. temperature transfer block) (column 3, lines 61-64 and column 4, lines 5-8), to the

surface of the device under test (column 5, lines 27-34). Suski also teaches connecting the Peltier device to a heat sink and corresponding fan (Figure 5).

While the invention of ESPEC, Nakayoshi, Agaya, and Suski teaches many of the features of the claimed invention, none of the prior art teaches or suggests, in combination with the other claimed limitations for testing internal components of an integrated circuit package device, the specific connections between the measuring components. More specifically, a computer means having a control program for connection and management of a controlled fan power supply, a programmable power supply, for controlling the addition of heat, by up-ramping, or reduction of heat, by down ramping, from the a temperature transfer block, and for sensing operations of a temperature meter and a digital multimeter.

- 2. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."
- 3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey R. West whose telephone number is (703)308-1309. The examiner can normally be reached on Monday through Friday, 8:00-4:30.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (703)308-1677. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7382 for regular communications and (703)308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

jrw January 9, 2004

MAT MARC STHOFF

SUPERMERBASORY PATENT EXAMINED

TECHTED MOLORY OUT (FR 2800)